

Assignment 6

1. In this assignment, we develop a behavioral model of a cyclic ADC and study the effect of non-idealities such as comparator offsets and gain errors on the ADC performance.

Ideal cyclic ADC

Construct an ideal 10-bit cyclic ADC capable of handling positive and negative signals with $V_{ref} = \pm 1V$. Use the sample and hold block from Assignment 1 to sample the input to the ADC. The cyclic operation is described by the flowchart seen in Lecture 6 with $V_{ref} = 2V$. Assign $+1.5V$ for logic 1 and $-1.5V$ for logic 0. Also, reconstruct the quantized signal at the output using the formula $V_{out} = \pm V_{ref} * (2^{-(i+1)})$ where b_i represents the output bits and b_0 is the MSB.

INL, DNL and SNR

Simulate the ADC with a ramp function and a clock frequency of 100 KHz such that input change is less than one LSB in one clock cycle. Import the reconstructed output into MATLAB and plot the INL, DNL and the reconstructed output. Do the results make sense?

Simulate the ideal ADC with a 10 KHz sinusoidal following the considerations used in Assignment 1. Choose the signal amplitude so that the ADC is not overloaded. Plot the spectra using the blackmanharris window and the code fragment used in Assignment 1. To determine the SNR, use the max function in MATLAB to determine the location of the input signal. Calculate the signal power by adding at least one point on both sides of the input signal including the input signal. Calculate the noise power by considering points up to $4 * f_{in}$ excluding the points constituting the signal power. Compute the SNR. How does it compare to the ideal SNR? Repeat the simulation using different input frequencies.

Now introduce the non-ideality described above into the ADC transfer function and re-plot the spectra. Compare this to the spectrum of the ideal ADC.

Non-ideal ADC behavior

Introduce an offset in the comparator threshold of 0.2V. Re-plot the INL, DNL and output spectrum. What do you observe? Now change the gain factor from 2 to 1.9 to model gain errors due to finite OTA gain, capacitor mismatch etc. Re-plot the INL, DNL and output spectrum. How much offset and gain error is tolerable for a 10-bit performance?

Two-tone test

Use the vsin component in Library analogLib to apply two signals at 10 KHz and 11 KHz at half the maximum amplitude for each tone. Plot the spectra and compute the dB ratio of the signal power to the power of the tones at $2 * f_2 - f_1$ and $2 * f_1 - f_2$ for the ideal ADC. Repeat the simulations for the non-idealities described above.