

## Assignment 8

1. In this assignment, we develop a behavioral model in VerilogA of a 1.5 bit per stage pipelined ADC and study the effect of comparator offsets on the ADC performance.

### Ideal 1.5 bit per stage pipelined ADC

Construct an ideal 10 bit 1.5 bit per stage pipelined ADC capable of handling positive and negative signals with  $V_{ref} = \pm 1V$ . Use the sample and hold block from Assignment 1 to sample the input to the ADC. Note that the last stage is a 2-bit ADC and we have a total of 9 stages with 18 digital bits. Perform digital error correction (shift and add) on the digital outputs to obtain the final 10 bits. Plot the INL and DNL of the ADC and verify its performance.

### Comparator offsets

Introduce offsets of +50mV, -200mV and +400mV on both the comparators in all stages. Plot the INL and DNL. What is the accuracy of the ADC in each case?

2. Consider a 10 bit 1.5 bit per stage pipelined ADC with  $V_{ref} = \pm 1V$ . The ADC is required to sample at 50 MS/s and should handle input signals up to a maximum frequency of 5 MHz. Calculate the following parameters for the first stage assuming a fully differential architecture.

- a) Input and sampling capacitors assuming a flip capacitor gain stage.
- b) Switch input resistance
- c) OTA gain, bandwidth, slew rate and input referred noise.
- d) Estimate the power dissipation assuming the same stage is repeated throughout the pipeline.